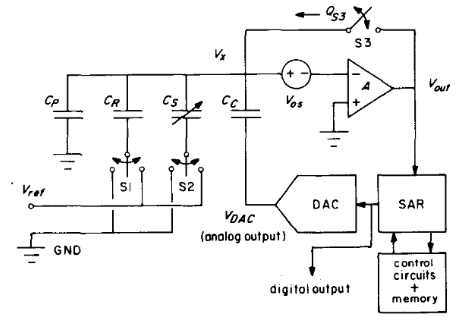
**Motivation and Introduction:**

The measurement of very small capacitances in integrated sensing circuits can be challenging due to the need for specialized detection circuitry. One current technique involves using an oscillator and a bridge circuit to detect changes in frequency caused by changes in reference capacitance. However, this method is affected by parasitic capacitance, which can lead to errors in measurement. A new technique known as switched capacitor techniques has been developed to improve capacitance detection, but it also suffers from limitations such as charge injection and circuit noise. This paper proposes a sensing technique that is based on the charge redistribution used in analog-to-digital converters, which is not affected by parasitic capacitance, offset in operational amplifiers or charge injection issues.

In Bullet points:

* Oscillatory and Bridge Circuit uses change in reference capacitance, Parasitic capacitance causes errors in measurements.
* Switched Capacitor Technique also suffers from Charge Injection, circuit noise and clock feedthrough.
* New Sensing technique based on charge redistribution used in A/D, not affected by parasitic capacitance, offset in op-amps or charge injection issues.

**Methodology and Observations:**



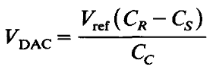
The proposed method uses a combination of a coupling capacitor (Cc), five MOS switches, a digital-to-analog converter (DAC), a successive approximation register (SAR), a voltage comparator, and a memory register with related logic to perform signal inversion.

Measurement is done as firstly with ideal system and then nonidealities like parasitic capacitance (Cp), Comparator Offset (Vos), Finite Gain (A) of the comparator and Switch Charge Injection (QS3) are added into the system.

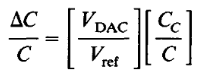
Measurement in Ideal system: It proceeds in two steps

Step 1: Switch S3 is closed, Switch S1 is set at Vref and Switch S2 is set at ground, The DAC output is also set to ground, The charge at Q1 is -VrefCR, the comparator is implemented so that the Vx is set to virtual ground via DAC.

Step 2: Switch S3 is now opened, Switch S1 set to ground and Switch S2 set to Vref, the SAR begins after this sequence and stops after it has reached its quantization limits, as the system is ideal so VDAC forces Vx to be zero and charge at the top node becomes Q2 = -VrefCS-VDACCC, by the charge conservation we get Q1=Q2, so



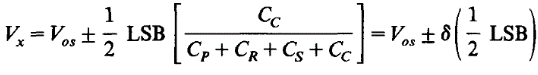
The output of the digital-to-analog converter is based on the capacitance difference between the CS and CR components. By selecting suitable values for Vref and CC, it is possible to optimize the usage of the full range of the DAC. can be found by multiplying numerator and denominator by CR ­­or CS.



Now the Nonidealities are added into the system such as Quantization Error, Charge Injection, Parasitic capacitance and other non-ideal effects.

1. Quantization Error

The measurement error caused by the DAC is due to the quantization error. If the output voltage of the DAC, VDAC, is off by ±1/2 least significant bit, the error that is transferred to VX can be represented by the equation

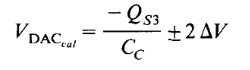


where is the ratio of the capacitors, any change in ∆V at VDAC will result in a change of ∆V at VX. In the worst-case scenario, this error will accumulate with each subsequent measurement, but averaging can help to reduce this problem.

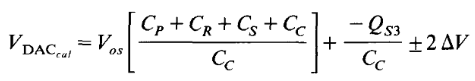
1. Charge Injection

An extra cycle will be added called as calibration cycle to measure the charge injected by the switch S3, the cycle of capacitive mismatch will be called measurement cycle, in closed loop topology the comparator offset is eliminated and in open loop topology the offset is measure and then cancelled.

The calibration cycle begins by measuring charge injection, S1 set to Vref, S2 and VDAC both set to ground and S3 is opened and SAR/DAC is initiated, and the voltage output is



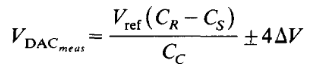
In closed loop and in open loop it is



Where V is the Quantization error of the DAC.

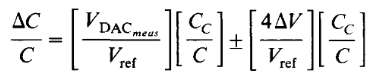
DAC creates a large positive charge enough at coupling capacitor to cancel the negative switch injection.

In measurement cycle,S3 is closed, S1 set to Vref, S2 set to ground and VDAC set to negative of the voltage measured in the calibration cycle, the switch cycle is same as in ideal system measurement, and the output is



1. Parasitic Capacitance

Parasitic capacitance can reduce the Capacitor ratio , VX is affected and DAC is not able to adjust. Smaller Cp increases the but also introduces kT/C noise so a trade off is introduced. The capacitive mismatch ratio for both topologies is



The precision of a single measurement is determined by this error term, which sets a limit on the smallest change in capacitance that can be distinguished. The presence of parasitic capacitance limits the accuracy of the comparator

1. Other Non-Ideal Effects

Even when a MOS switch is turned off, a small amount of current can still leak through the reverse-biased p-n junction. This leakage is relatively insignificant, but at low frequencies and high temperatures, it can become more pronounced. This leakage current can be measured at low frequencies. The test capacitors used in this measurement tend to have similar temperature coefficients, which can cause a common mode error that cancels out in differential measurements. Additionally, thermal noise generated during the measurement process can cause variations in the injection charge each time switch S3 is opened.



Increasing the value of the sense and reference capacitors, C, can help to reduce noise in the measurement, but it also increases the parasitic capacitance. When the sense and reference capacitors are already small, it is not possible to completely eliminate the effect of parasitic capacitance through a single measurement. However, by using digital averaging techniques, it is possible to reduce the impact of parasitic capacitance as the noise is random in nature.

Observations:

A test chip was fabricated using 3-micrometer p-well CMOS technology by MOSIS and was used to demonstrate various measurements of metal/poly capacitors that were comparable. The Open Loop topology was implemented during the design process. Five chips were obtained per run, with test capacitors ranging from 20-100 fF.

A calibration test was conducted 100 times and then averaged and the negative of the average value was then applied to CC and the calibration cycle was repeated, resulting in a DAC output near zero, which showed successful noise reduction. The residual polarization was found to be insignificant. The slight discrepancy in standard deviations between the negative and positive measurements is caused by slight asymmetrical noise coupling control signals to the test chip.

It was observed that the difference between small capacitors was very minimal, on the order of 0.1-1 percent. The resolution limit was achieved by averaging over 16 times. The resolution of a single measurement was found to be close to 1000-1500 electrons which is nearly 0.05 fF. Different sequences will produce varying results, and the designer can use the sequence that is most suitable for the specific application.

Conclusion:

A method was successfully demonstrated for measuring small differences in capacitance with a resolution of 0.05 femtofarads (fF) on capacitors in the range of 20-100 fF, even in the presence of parasitic capacitance that is nearly 100 times larger. The paper also showed that nonideal effects can be corrected through calibration and that digital averaging can improve resolution, but at the cost of longer measurement times. This technique improves upon previous designs and is useful in sensor systems.